52B13/52B13H

E^2 16K Electrically Erasable ROM

PRELIMINARY DATA SHEET

August 1984

Features

- Input Latches
- TTL Byte Erase/Byte Write
- 1 ms (52B13H) or 9 ms Byte Erase/Byte Write
- Power Up/Down Protection
- 10,000 Erase/Write Cycles per Byte
- 5V ± 10% Operation
- Fast Read Access Time — 200 ns
- Infinite Number of Read-Cycles
- Chip Erase and Byte Erase
- DiTrace™
- JEDEC Approved Byte Wide Memory Pinout

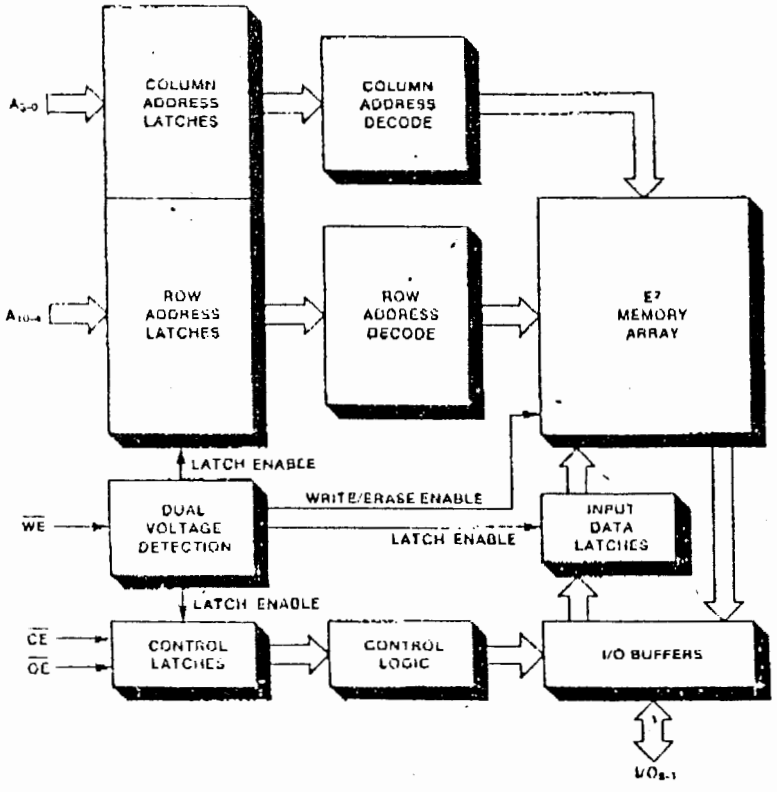
Description

SEEQ's 52B13 and 52B13H are 2048 x 8 bit, 5 volt electrically erasable, read only memories (E^2ROM) with input latches on all address, data and control (chip and output enable) lines. Data is latched and electrically written by either a TTL or a 21V (52B13 only) pulse on the Write Enable pin. Once written, which requires under 10 ms, there is no limit to the number of times data may be read. Both byte and chip erase modes are available. The erasure time in either mode is under 10 ms, and each byte may be erased and written up to 10,000 times. They are direct pin-for-pin replacement for SEEQ's 5213.

The 52B13 and 52B13H are ideal for applications that require a non-volatile memory with in-system write and erase capability. Dynamic reconfiguration (the alteration of operating software in real-time) is made possible by this device. Applications for the 52B13 and 52B13H will be found in military avionics systems, programmable character generators, self-calibrating instruments/

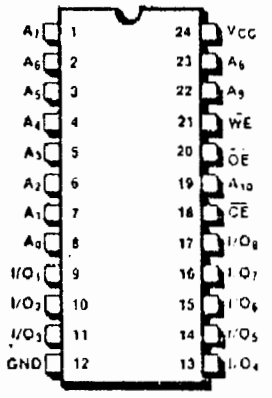
(continued on page 2)

Block Diagram



Pin Configuration

52B13/52B13H



Pin Names

A_0-A_{10}	ADDRESSES
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
I/O	DATA INPUT (WRITE OR ERASE) DATA OUTPUT (READ)

machines, programmable industrial controllers, and an assortment of other systems. Designing the 52B13 and 52B13H into eight and sixteen bit microprocessor systems is also simplified by utilizing the fast access time with zero wait states. The addition of the latches on all data, address and control inputs reduces the overhead on the system controller by eliminating the need for the controller to maintain these signals. This reduces IC count on the board and improves the system performance. Extended temperature and military grade versions are available.

Device Operation

SEEQ's 52B13 and 52B13H have six modes of operation (see Table 1) and except for the chip erase mode they require only TTL inputs to operate these modes.

To write into a particular location of the 52B13 or 52B13H, that byte must first be erased. A memory location is erased by presenting the 52B13 or 52B13H with Chip Enable at a TTL low while Output Enable is at TTL high, and TTL highs (logical 1s) are being presented to all the I/O lines. These levels are latched and the data written when write enable is brought to a TTL low level. The erase operation requires under 10 ms. A write operation is the same as an erase except true data is presented to the I/O lines. The 52B13H performs the same as the 52B13 except that the device operates at 5 volts only and the byte erase/byte write time has been enhanced to 1 ms.

The 52B13 is compatible to prior generation E²ROMs which required a high voltage signal for writing and erasing. In the 52B13 there is an internal dual level detection circuit which allows either a TTL low or 21V signal (52B13 only) to be applied to $\overline{WE}$ to execute an erase or write operation. The 52B13 specifies no restriction on the rising edge of $\overline{WE}$.

For certain applications, the user may wish to erase the entire memory. A chip erase is performed in the same manner as a byte erase except that Output Enable is between 14V and 22V. All 2K bytes are erased in under 10 ms.

A characteristic of all E²ROMs is that the total number of write and erase cycles is not unlimited. The 52B13 and 52B13H have been designed for applications requiring up to 10,000 write and erase cycles per byte. The write and erase cycling characteristic is completely byte independent. Adjacent bytes are not affected during write/erase cycling.

After the device is written, data is read by applying a TTL high to $\overline{WE}$, enabling the chip, and enabling the outputs. Data is available t_{CE} time after Chip Enable is applied or t_{ACC} time from the addresses. System power may be reduced by placing the 52B13 or 52B13H into a standby mode. Raising Chip Enable to a TTL high will reduce the power consumption by over 60%.

DiTrace™

SEEQ's family of E²ROMs incorporate a DiTrace™ field. The DiTrace™ feature is a method for storing production flow information to wafer level in an extra column of E²ROM cells. As each major manufacturing operation is performed the DiTrace™ field is automatically updated to reflect the results of that step. These features establish manufacturing operation traceability of the packaged device back to the wafer level. Contact SEEQ for additional information on these features.

Table 1. Mode Selection (V_{CC} = 5V ± 10%)

Mode \ PIN	$\overline{CE}$ (18)	$\overline{OE}$ (20)	$\overline{WE}$ (21)	I/O (9-11, 13-17)
Read[1]	V_{IL}	V_{IL}	V_{IH}	DOUT
Standby[1]	V_{IH}	Don't Care	V_{IH}	High Z
Byte Erase[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN} = V_{IH}
Byte Write[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Chip Erase[2]	V_{IL}	V_{OE}	V_{IL}	D_{IN} = V_{IH}
Write/Erase Inhibit	V_{IH}	Don't Care	Don't Care	High Z

Notes:
1. $\overline{WE}$ may be from V_{IH} to 0V in the read and standby mode.
2. $\overline{WE}$ may be at V_{IH} (TTL WE Mode) or from 19V to 22V (High Voltage WE Mode) in the byte erase, byte write, or chip erase mode of the 52B13.

52B13/52B13H Specification Differences

Except for the functional differences noted here, the 52B13 and 52B13H operate to the same specifications including the TTL W.E mode

Symbol	Function/Parameter	52B13		52B13H		Units
		Min.	Max.	Min.	Max.	
t_{WP}	Write Enable Pulse Width					
	Byte Write/Erase	9	70	1	10	ms
	Chip Erase	9	70	9	20	ms
V_{WE}	$\overline{WE}$ Write/Erase Voltage High Voltage Mode	15	22	Not Applicable		V

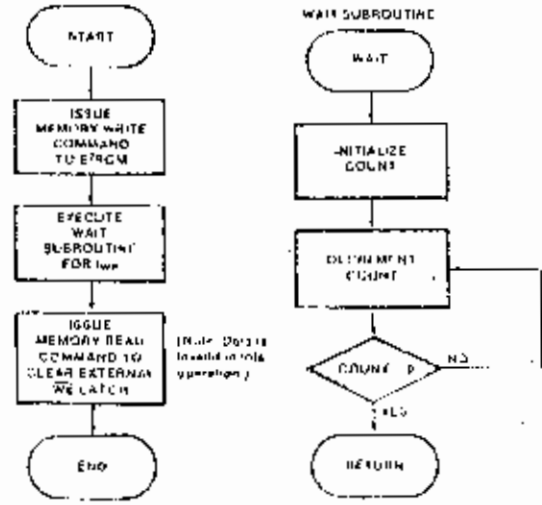
Power Up/Down Considerations

SEEQ's "52B" E^2 family has internal circuitry to minimize false erase or write during system V_{CC} power up or down. This circuitry prevents writing or erasing under any one of the following conditions:

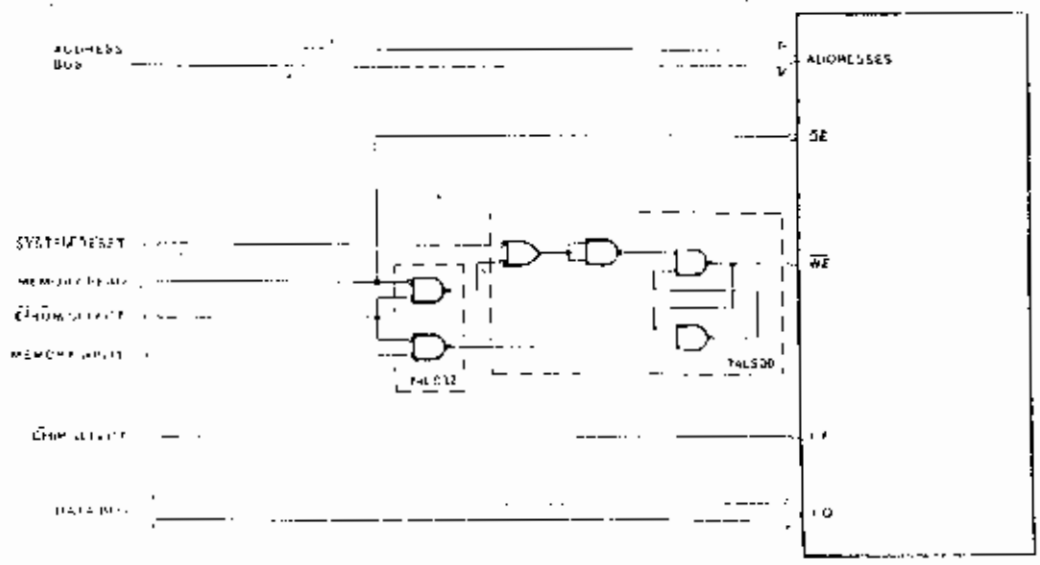
1. *V_{CC} is less than 3 V*
2. *A negative Write Enable transition has not occurred when V_{CC} is between 3 V and 5 V.*

Writing will also be prevented if $\overline{CE}$ or $\overline{OE}$ are in a logical state other than that specified for a byte write in the mode selection table.

Typical E^2ROM Write/Erase Routine



Microprocessor Interface Circuit Example for Byte Write/Erase



Absolute Maximum Stress Ratings*

Temperature
Storage ..... -65° C to +150° C
Under Bias ..... -10° C to +80° C
All Inputs or Outputs with Respect to Ground ..... +6V to -0.3V
WE During Writing/Erasing with Respect to Ground ..... -22.5V to -0.3V
Duration of WE Supply at 22V During WE Inhibit ..... 24 Hours

**COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

Recommended Operating Conditions

	52B13-200/-250/-350 52B13H-200/-250/-350
V_{CC} Supply Voltage	5 V ±10%
Temperature Range	0° C to 70° C
Q (Minimum Endurance)[3]	10,000 cycles/byte

D.C. Operating Characteristics During Read or Write/Erase (Over the operating V_{CC} and temperature range)

Symbol	Parameter	Min.	Nom.[1]	Max.	Unit	Test Conditions
I_{LI}	Input Leakage Current			10	µA	$V_{IN} = V_{CC}$ Max
I_{LO}	Output Leakage Current			10	µA	$V_{OUT} = V_{CC}$ Max
I_{WE}	Write Enable Leakage					
	Read Mode			10	µA	$\overline{WE} = V_{IH}$
	TTL W/E Mode			10	µA	$\overline{WE} = V_{IL}$
	High Voltage W/E Mode[2]			1.5	mA	$WE = 22V$, $\overline{CE} = V_{IL}$
	High Voltage W/E Inhibit Mode[2]			1.5	mA	$\overline{WE} = 22V$, $\overline{CE} = V_{IH}$
	Chip Erase — TTL Mode			10	µA	$\overline{WE} = V_{IL}$
	Chip Erase — High Voltage Mode[2]			1.5	mA	$WE = 22V$
I_{CC1}	V_{CC} Standby Current		15	30	mA	$\overline{CE} = V_{IH}$
I_{CC2}	V_{CC} Active Current		50	80	mA	$\overline{CE} = \overline{OE} = V_{IL}$
V_{IL} (D.C.)	Input Low Voltage (D.C.)	-0.5		0.8	V	
V_{IL} (A.C.)	Input Low Voltage (A.C.)	-0.4			V	Time = 10 ns
V_{IH}	Input High Voltage	2		V_{CC} + 1	V	
V_{WE}	WE Read Voltage	2		V_{CC} + 1	V	
	WE Write/Erase Voltage					
	TTL Mode	-0.1		0.8	V	
	High Voltage Mode[2]	14		22	V	
V_{OL}	Output Low Voltage			0.45	V	$I_{OL} = 2.1$ mA
V_{OH}	Output High Voltage	2.4			V	$I_{OH} = -400$ µA
V_{CE}	$\overline{OE}$ Chip Erase Voltage	14		22	V	$I_{OE} = 10$ µA

Notes:
1. Nominal values are for T_A = 25° C and V_{CC} = 5.0V.
2. Not applicable to 52B13H.
3. Each Byte may be written or erased over the temperature and V_{CC} range up to the recommended endurance (Q) specification.

A.C. Operating Characteristics During Read (Over the operating V_{CC} and temperature range)

Symbol	Parameter	Device Number Extension	52B33 52B33H Min.	52B33 52B33H Max.	Unit	Test Conditions
t_{ACC}	Address to Data Valid	-200		200	ns	$\overline{CE} = \overline{OE} = V_{IL}$
		-250		250	ns	
		-350		350	ns	
t_{CE}	Chip Enable to Data Valid	-200		200	ns	$\overline{OE} = V_{IL}$
		-250		250	ns	
		-350		350	ns	
t_{OE} [1]	Output Enable to Data Valid	-200	10	80	ns	$\overline{CE} = V_{IL}$
		-250	10	90	ns	
		350	10	100	ns	
t_{DF} [2]	Output Enable to High Impedance	-200	0	60	ns	$\overline{CE} = V_{IL}$
		-250	0	70	ns	
		-350	0	80	ns	
t_{OH}	Output Hold	All	0		ns	$\overline{CE} = \overline{OE} = V_{IL}$

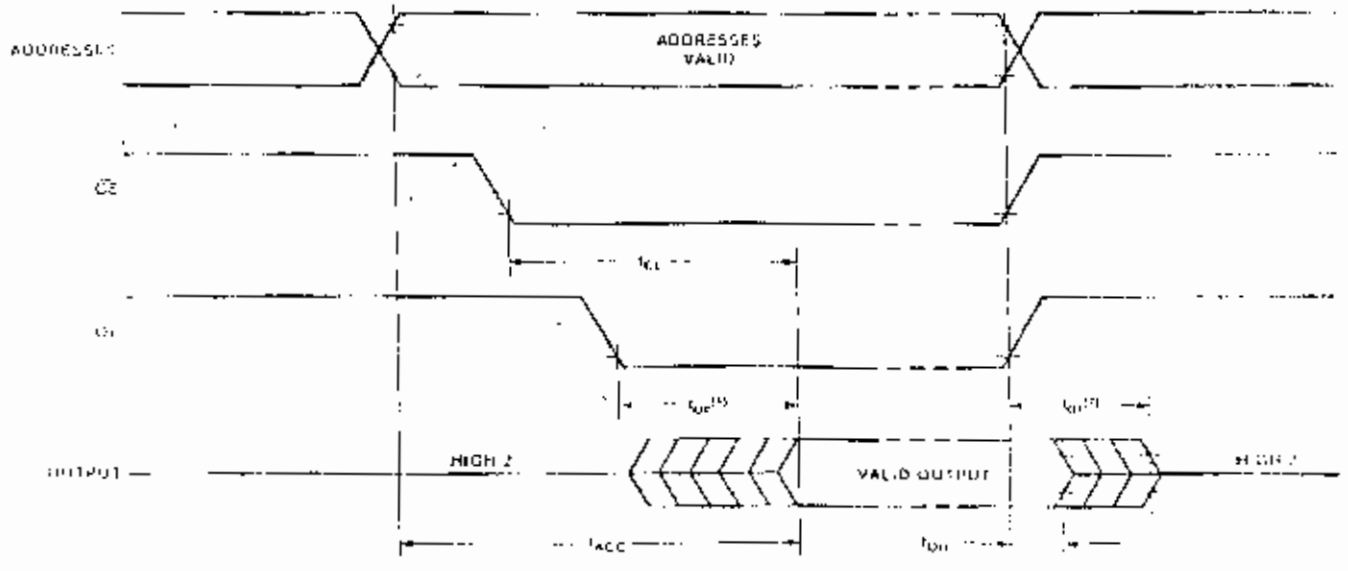
Capacitance[3], T_A = 25°C, f = 1MHz

Symbol	Parameter	Max.	Unit	Conditions
C_{IN}	Input Capacitance	10	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance	10	pF	V_{OUT} = 0V
C_D	V_{CC} Capacitance	500	pF	$\overline{OE} = \overline{CE} = V_{IH}$
C_{WE}	V_{WE} Capacitance	10	pF	$\overline{OE} = \overline{CE} = V_{IH}$

A.C. Test Conditions

Output Load: 1 TTL gate and C_L = 100 pF
Input Rise and Fall Times: ≤ 20ns
Input Pulse Levels: 0.45V to 2.4V
Timing Measurement Reference Level:
Inputs 1V and 2V
Outputs 0.8V and 2V

Read Timing



Notes:
1. t_{OE} may be delayed up to t_{CE} - t_{OE} after the falling edge of $\overline{CE}$ without impact on t_{ACC}.
2. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.
3. This parameter is periodically sampled.

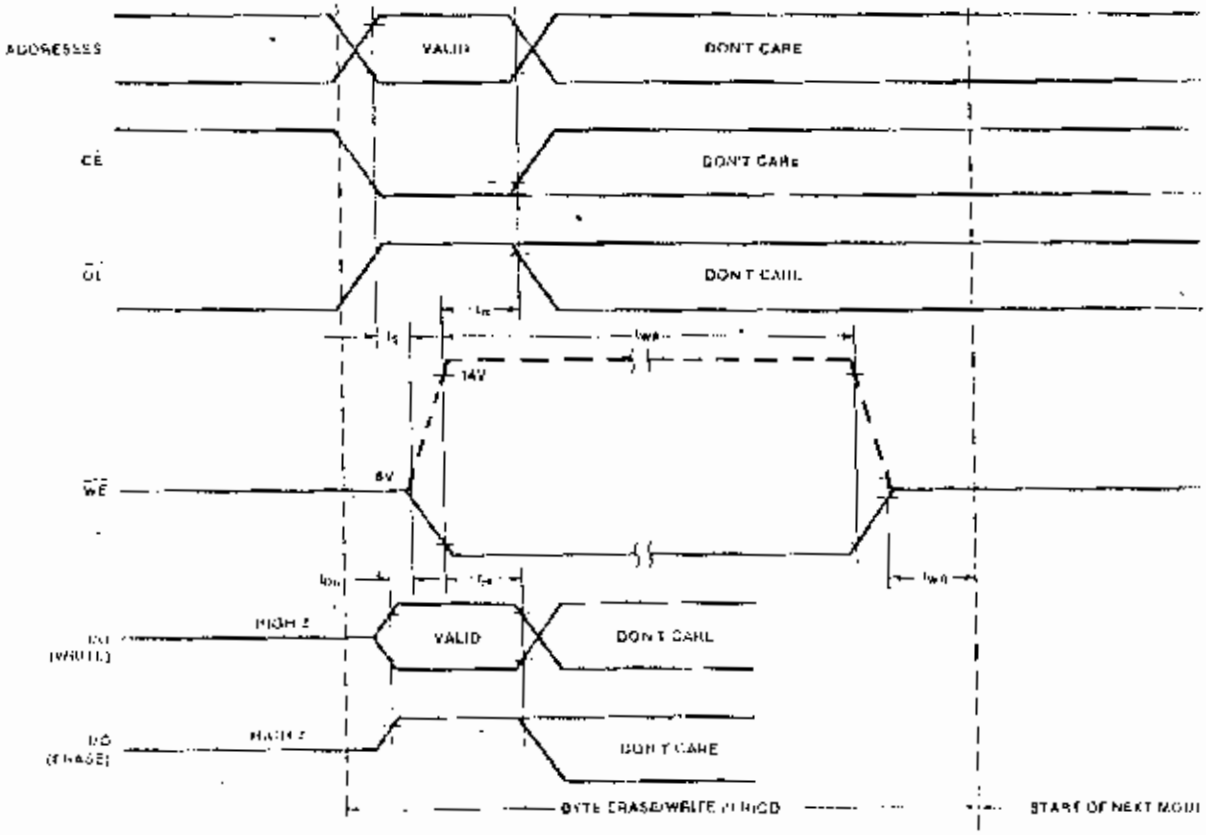
A.C. Operating Characteristics During Write/Erase (Over the operating V_{CC} and temperature range)

Symbol	Parameter		Min.	Max.	Units
t_S	$\overline{CE}$, $\overline{OE}$ or A_N Setup to $\overline{WE}$		50		ns
t_{DS}	Data Setup to $\overline{WE}$		0		ns
t_H[1]	$\overline{WE}$ to $\overline{CE}$, $\overline{OE}$, A_N or Data Change		50		ns
t_{WE}	Write Enable, $\overline{WE}$, Pulse Width	52B13	9		ms
		52B13H	1		ms
t_{WR}[2]	$\overline{WE}$ to Mode Change		50		ns

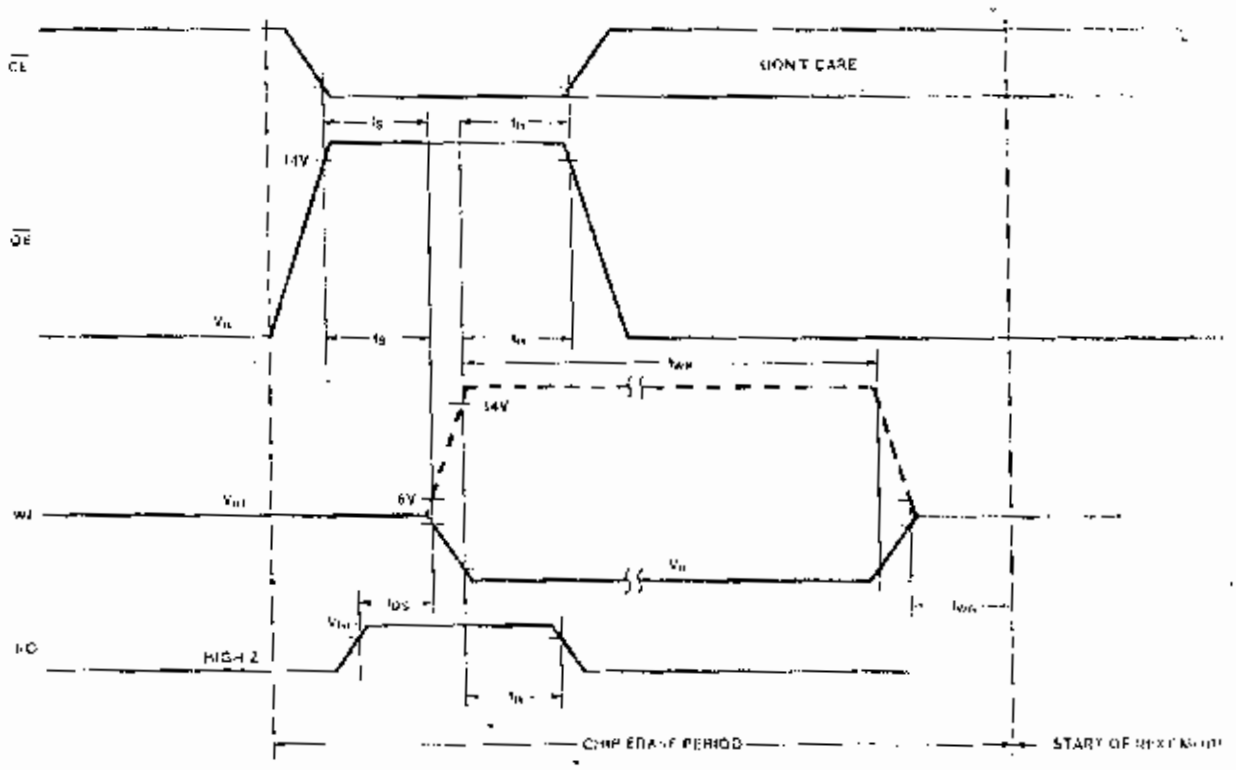
Notes

1. After t_H hold time, from $\overline{WE}$, the inputs $\overline{CE}$, $\overline{OE}$, Address and Data are latched and are "Don't Cares" until t_{WR} write recovery time after the trailing edge of $\overline{WE}$.
2. For Write Recovery Time, t_{WR}, is the time after the trailing edge of $\overline{WE}$ that the latches are open and able to accept the next mode control conditions. Reference Table 1, page 2, for mode control conditions.

Byte Erase or Byte Write Timing



Chip Erase Timing



Ordering and Packaging Information

PART NUMBERS

DQ52B13 350

DQ52B13H 350

ACCESS TIME (ns)

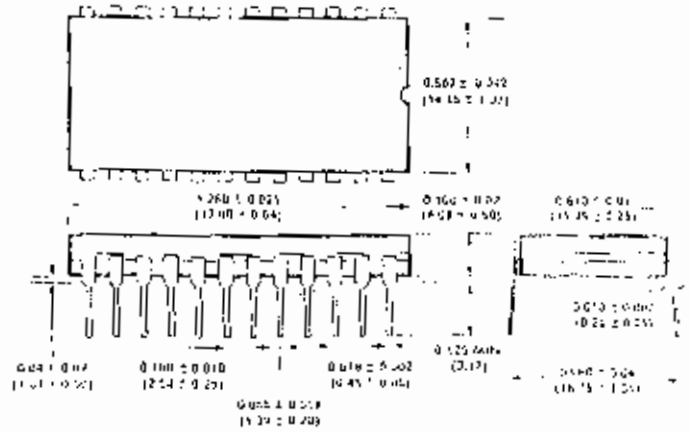
5 ms WRITE TIME AND 5V ONLY

PROGRAMMABLE EPROM

TEMPERATURE RANGE 0°C to 70°C

PACKAGE: CERDIP

24-LEAD HERMETIC CERDIP
PACKAGE TYPE D



DIMENSIONS IN INCHES AND (MILLIMETERS)